Remarks

Claims 1-11 are currently pending in the patent application. For the reasons and arguments set forth below, Applicant respectfully submits that the claimed invention is allowable over the cited references.

The Office Action dated December 17, 2007 notes an objection to the specification and the following rejections: claims 1, 3 and 6-8 stand rejected under 35 U.S.C. § 103(a) over Krakauer *et al.* (US Patent No. 5,617,283) in view of Ker *et al.* (US Patent Pub. 2002/0050615); claims 2 and 11 stand rejected under 35 U.S.C. § 103(a) over Krakauer in view of Ker and further in view of Lai *et al.* (US Patent Pub. 2003/0235022); claim 4 stands rejected under 35 U.S.C. § 103(a) over Krakauer in view of Ker and further in view of Yu *et al.* (US Patent No. 6,031,405); claim 5 stands rejected under 35 U.S.C. § 103(a) over Krakauer in view of Ker and Yu and further in view of Ulmer (US Patent No. 4,612,497); claim 9 stands rejected under 35 U.S.C. § 103(a) over Krakauer in view of Ker and further in view of Ker *et al.* (US Patent No. 6,912,109, hereinafter Ker '109); and claim 10 stands rejected under 35 U.S.C. § 103(a) over Krakauer in view of Ker and further in view of Narita (US Patent No. 5,973,901).

Applicant appreciates the Examiner's attention to the specification. Regarding the informality on page 6, Applicant has amended the specification to reflect that the protection circuit refers to FIG. 2. Regarding the arrangement of the specification, Applicant respectfully declines to add section headings because the indicated suggestions in 37 C.F.R. § 1.77(b) are not statutorily required for filing a non-provisional patent application under 35 USC § 111(a), but per 37 C.F.R. § 1.51(d) are only guidelines that are suggested for applicant's use. They are not mandatory, and when Rule 77 was amended in 1996 (61 FR 42790, Aug. 19, 1996), Bruce A. Lehman, Assistant Secretary of Commerce and Commissioner of Patents and Trademarks, stated in the Official Gazette:

> "Section 1.77 is permissive rather than mandatory. ... 1.77 merely expresses the Office's preference for the arrangement of the application elements. The Office may advise an applicant that the application does not comply with the format set forth in 1.77, and suggest this format for the applicant's consideration; however, the Office will not require any application to comply with the format set forth in 1.77."

In view of the above, Applicant prefers not to add section headings.

Applicant respectfully traverses all of the Section 103 rejections, each of which relies upon a combination of Ker with Krakauer, because the asserted combination does not provide teaching or suggestion of all of the claim limitations including those directed to a time-delay means for connecting between a supply voltage terminal and transistor control inputs. Furthermore, the asserted motivation is misplaced because the cited portions of the secondary Ker reference do not function as suggested. The following addresses each of these issues separately.

The cited ESD detection circuit 86 from FIG. 6b of the Ker reference is not, as suggested in the Office Action, "time delay means connected between a supply voltage terminal and [first and second transistors]." Specifically, the ESD detection circuit in Ker's FIG. 6b includes a resistor (R) and capacitor (C), with a node between the resistor and capacitor coupled to an input of a pSCR (a PMOS triggered low-voltage-triggered semiconductor controlled rectifier). The connection of the node between the resistor (R) and capacitor (C) to the pSCR is to "drive the control gate to a relative-low voltage to trigger the PSCR and conduct ESD current" (*see, e.g.*, paragraph 0037, lines 4-18). The output of the capacitor (C) is connected directly to an I/O pad 80. In this regard, the alleged "time delay means" 86 is coupled between a power supply (VDD) and an I/O pad 80, and only the resistor (R) is coupled between VDD and a control input.

Ker's ESD detection circuit 86 therefore does not correspond to limitations in claim 1 directed to time-delay means connected between a supply voltage terminal and control inputs of first and second transistors, where the transistors are coupled between the time-delay means and a pad. Moreover, it appears that Ker's ESD detection circuit 86 would circumvent the protection characteristics of the claim limitations, in that the output of the capacitor (C) is coupled directly to an I/O pad (*see, e.g.*, FIG. 6b), and thus cannot provide correspondence to the claimed invention. See, for example, claim 1 of the instant invention and the example embodiments shown in FIG. 2.

In view of the above, the Section 103(a) rejection of claim 1 fails to provide teaching or suggestion of all of the claim limitations. As claims 2-11 depend from claim 1, the Section 103(a) rejections of these claims accordingly also fail to provide teaching or suggestion of all of the claim limitations. Notwithstanding this, the proposed combination of references also fails to teach or suggest various limitations in the dependent claims. For instance, regarding claims 3 and 4, Ker's ESD detection circuit 86

is not adapted for connection in series to any control input of a transistor or otherwise. Rather, as discussed above, a node between the resistor (R) and capacitor (C) is connected to the control input of a pSCR device, rather than in series to such a control input. Regarding claim 7, the cited portion of the Krakauer reference appears to reference a single transistor, and does not provide any teaching of second, third and fourth transistors connected as claimed.

In addition to the above, there is no motivation to modify Krakauer with Ker's ESD detection circuit 86 to arrive at the claimed invention because, as discussed above, Ker's ESD detection circuit is connected directly to its I/O pad 80. This, when used to modify Krakauer, would result in connecting directly to Krakauer's I/O pad and, accordingly, would circumvent the protective characteristics of Krakauer's circuit (and the claimed invention). For example, applying Ker to Krakauer would appear to involve somehow using the node between Ker's resistor (R) and capacitor (C) in its ESD detection circuit 86 to control an input of a transistor. That is, while Ker shows a resistor and capacitor in series, the circuit as a whole teaches away from the claimed invention (and modification of Krakauer to arrive at the same) in that it controls a pSCR using a node *between* RC elements, rather than in series with such elements, and is further directly connected to an I/O pad. In this regard, it is unclear as to how the Krakauer reference could function using an RC circuit arranged as disclosed in Ker. Therefore, the Office Action's suggestion that one of skill in the art would be motivated by Ker to modify Krakauer in a manner that is completely different than the teachings in Ker (to arrive at the claimed invention) is untenable. Applicant submits that there is therefore no motivation to modify Krakauer with Ker as suggested in the Office Action.

Regarding claims 2, 4-5 and 9-11, while the Office Action turns to multiple additional references in an attempt to show correspondence to the claim limitations, Applicant submits that these combinations fail for the reasons cited above, in both failing to provide adequate teaching or suggestion of all of the claim limitations, or motivation for combining the cited references. In this regard, further discussion of these rejections is omitted for brevity. However, Applicant traverses the rejections of these claims and their proposed combinations, and reserves the right to address the same should any rejections be maintained.

In view of the above, the Section 103(a) rejections of all of the claims fail to establish *prima facie* obviousness, based upon either a teaching or suggestion of all limitations or a showing of motivation for modifying the primary Krakauer reference to arrive at the claimed invention. Applicant therefore requests that the Section 103(a) rejections, each of which relies upon the combination of Ker with Krakauer, be removed.

New claims 12-15 should be allowable over the cited references for the reasons stated above. For instance, the cited references fail to disclose related limitations in claim 1, and limitations in new independent claim 12 such as those directed to a time-delay circuit including a resistor and a capacitive device connected in series, the resistor being connected to a power supply and the capacitive device being connected to control inputs of first and second transistors. New claims 13-15 depend from claim 12 and therefore include these limitations as well.

Claim 1 has been amended for readability and flow. Claim 7 has been amended to correct dependency (in reciting third and fourth transistors, which are not present in claim 1 but present in claim 5). These amendments were not made in view of any prior art, cited herein or otherwise.

In view of the above, Applicant believes that each of the rejections has been overcome and the application is in condition for allowance. Should there be any remaining issues that could be readily addressed over the telephone, the Examiner is asked to contact the agent overseeing the application file, Peter Zawilski, of NXP Corporation at (408) 474-9063.

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